Amendments to the Claims:

This listing of the claims replaces all prior versions and listing of the claims in the present application.

Listing of Claims:

1. (currently amended) A multi-phase clock generation circuit comprising:

reference clock signal generation means for generating 2^n (n is a positive integer) reference clock signals having the same frequency, the plurality of reference clock signals having different phases;

first frequency division means for frequency-dividing one of the plurality of reference clock signals from said reference clock signal generation means [[by 2]] to generate first and second clock signals [[180°]] out of phase with each other on the basis of frequency division outputs;

first clock selection means for selecting one of each of the first and second clock signals from said first frequency division means and ~~a corresponding~~ one of the reference clock ~~signal~~ signals and outputting the selected signals as first and second clock pulses;

second ~~to nth~~ frequency division means for ~~each of which frequency divides a~~ frequency-dividing one of the clock ~~pulse~~ pulses from said first clock selection means to generate ~~$(2^m - 1)$th to $(2^{m+1} - 2)$th (m is a positive integer of not less~~

~~than 2)~~ third through sixth clock signals [[180°]] out of phase with each other on the basis of frequency division outputs;

second ~~to nth~~ clock selection means ~~each of which selects~~ for selecting one of each of the third through sixth clock signals from said second ~~to nth~~ frequency division means and ~~a corresponding~~ one of the reference clock signals to output the selected signals as ~~$(2^m - 1)$th to $(2^{m+1} - 2)$th~~ third through sixth clock pulses; and

clock selection control means for controlling said first ~~to nth~~ and second clock selection means in accordance with a set frequency division ratio.

2. (original) A circuit according to claim 1, wherein said clock selection control means comprises frequency division number setting means for setting a frequency division number for a clock signal output from predetermined clock selection means.

3. (currently amended) A circuit according to claim 1, wherein

said circuit further comprises first-stage frequency division means for generating a clock signal from an arbitrary one of the plurality of reference clock signals, and

said first frequency division means generates first and second clock signals [[180°]] out of phase with each other by frequency-dividing the generated clock signal [[by 2]].

4. (currently amended) A circuit according to claim 1, wherein

each of said first to [[nth]] second frequency division means comprises D flip-flop circuits and inverters.

5. (original) A circuit according to claim 4, wherein an output terminal of a predetermined D flip-flop circuit of the D flip-flop circuits is connected to an input terminal of another D flip-flop circuit forming said frequency division means.

6. (original) A circuit according to claim 5, wherein a clock signal output from a predetermined D flip-flop circuit and a clock signal input to another D flip-flop circuit have the same timing.

7. (currently amended) A circuit according to claim 1, further comprising clock shut-off means for shutting off at least some of clocks input to said first to [[nth]] second clock selection means which are not in use.

8. (original) A circuit according to claim 3, wherein said first-stage frequency division means comprises

a D flip-flop circuit, and

an inverter.

9. (original) A circuit according to claim 1, wherein said reference clock signal generation means comprises a PLL circuit.

10. (original) A circuit according to claim 1, further comprising reference clock signal selection means for selecting an arbitrary reference clock signal of the plurality of reference clock signals which is input to said first frequency division means.

11. (original) A circuit according to claim 3, further comprising reference clock signal selection means for selecting an arbitrary reference clock signal of the plurality of reference clock signals which is input to said first-stage frequency division means.

12. (currently amended) A multi-phase clock generation circuit comprising:

reference clock signal generation means for generating 2^n (n is a positive integer) reference clock signals having the same frequency, the plurality of reference clock signals having different phases;

first to nth frequency division means each of which frequency-divides one of ~~an input~~ the reference clock ~~signal and a clock by 2~~ signals to generate $(2^p - 1)$th to $(2^{p+1} - 2)$th (p is a positive integer that is the number of the frequency division means ~~of not less than 1~~) clock signals [[180°]] out of phase with each other on the basis of frequency division outputs;

first to nth clock selection means each of which selects at least one of ~~each of~~ the clocks ~~signal~~ signals from

said first to nth frequency division means and ~~a corresponding~~ at least one of the reference clock signals to output the selected singals as $(2^p - 1)$th to $(2^{p+1} - 2)$th clock pulses; and

clock selection control means for controlling said first to nth clock selection means in accordance with a set frequency division ratio.